

Template for Special Session Proposal

Title FPGA design for IoT and AI applications

Session organizers

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Wajdi ELHAMZI is an assistant professor in computer engineering at the College of Computer Engineering and Sciences, Prince Sattam bin Abdulaziz University, Al-Kharj, Saudi Arabia. He received his Ph.D. from the University of Burgundy, France in 2013 and a PhD in electronics and microelectronics from the University of Monastir, Tunisia the same year. Elhamzi is conducting research in Hardware design, with an emphasis on topics related to Artificial intelligence, image processing, and lightweight cryptography, such as medical image segmentation and classification, watermarking, and hardware accelerator design based on FPGA circuits.

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Dr. Mohamed EL-HADEDY is an Associate Professor and the Director of the Reconfigurable Space Computing Laboratory at the Electrical and Computer Engineering Department, Cal Poly Pomona. He also holds roles as a Visiting Research Scientist at the Coordinated Science Laboratory at UIUC and a Summer Faculty Fellow at the USAFA under the AFRL Summer Research Program. With several U.S. patents in reconfigurable computing, Dr. El-Hadedy's research advances computational technologies for space systems, contributing extensively to the field through numerous publications. His academic and professional work is recognized for its impact on developing adaptive technologies that meet the rigorous demands of aerospace applications.

• Dr. Kamel MESSAOUDI, <u>k.messaoudi@univ-soukahars.dz</u>

Associate professor in the department of electronics, Souk Ahras University, Algeria.

Dr. Kamel MESSAOUDI received an engineering degree in automatic from the University of Annaba, Algeria (1997), and a master's degree in Industrial Computing and image processing from the University of Guelma, Algeria (2000). He received his Ph.D. degree in electronics from Badji Mokhtar University, Annaba (2012), and a Ph.D. degree in instrumentation and image processing from Burgundy University Dijon, France (2012). He is an associate professor in the Department of Electronics, at Souk Ahras University, Algeria. His research interests include Image processing, embedded systems, FPGA design, and Real-time implementation.

Brief Description of the session thematic

Field-Programmable Gate Arrays (FPGAs) are versatile hardware platforms capable of being reprogrammed to address a broad spectrum of tasks, making them ideal for Internet of Things (IoT) and Artificial Intelligence (AI) applications. These devices excel in facilitating rapid development and enhanced performance of AI-driven tasks. Within the realm of IoT and AI, FPGA designers leverage these adaptable chips to prototype and refine various algorithms swiftly, enabling the efficient testing and optimization of designs before committing to a fixed hardware setup.

Today, there are several applications in which AI plays an offensive or defensive role in hardware security and a crucial role in predictive modelling for VLSI designs. The use of artificial intelligence techniques, such as machine learning (ML) and deep learning (DL), to build countermeasures against hardware threats. One of the most notable benefits of ML techniques is the automation of the attack detection process.

AI approaches, like as genetic algorithms and evolutionary learning, can be applied to improve different elements of VLSI architecture. Furthermore, AI aids in identifying important routes and reducing power usage in VLSI. AI can help improve approaches such as frequency scaling and dynamic voltage.

Indeed, AI can automate tasks such as datapath optimization and resource allocation. As a result, ML algorithms can understand design specifications, performance targets, and so on, which aids in the optimization of register transfer level (RTL).

Topics and Keywords

- FPGA design for Machine Learning and Artificial Intelligence
- FPGA design for IoT and Smart Systems
- AI based Hardware Security
- AI based VLSI Circuits Design

Number of pages

4 to 6 pages

Deadlines

Full paper submission: Paper acceptance notification: Camera-ready paper submission:

List of potential reviewers

- Dr. Anas Salah Eddin, Cal Poly Pomona, USA, asalaheddin@cpp.edu
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Submissions Procedure

The instructions for the submission of are included in the conference website through the following link: <u>https://icaige.recherche-scientifique.com/</u>



